Instrument Front-End Module

GLIDE

FEATURES

- LPC2468 PQFP208 72MHz
- 256 MB NAND FLASH, 4 MB NOR FLASH + 512 KB internal
  32 MB SDRAM + 96 KB internal
- 16-bit data bus to SDRAM and to expansion bus
- SD/MMC card connector full size
- 12.000 MHz crystal for CPU
- 32.768 kHz crystal for RTC
- USB Power, LiION, +5V
- Standard JTAG connector
- 7 User keys
- Touch-screen controller
- QVGA (16bit 320x240) TFT display, located on expansion bus for the maximum speed
- Speaker
- Step-Up DC-DC converter 1A +5V
- LiION charger
- Small size 90x90mm (HxV)
- Free ARMD IDE environment for C language
- Free GPACK utility for GUI interface
- Free libraries for SD,TFT,ARM,etc.

Embedded Camera

APPLICATIONS

- Portable instruments
- Embedded cameras
- Robotics
- Remote instruments

GENERAL DESCRIPTION

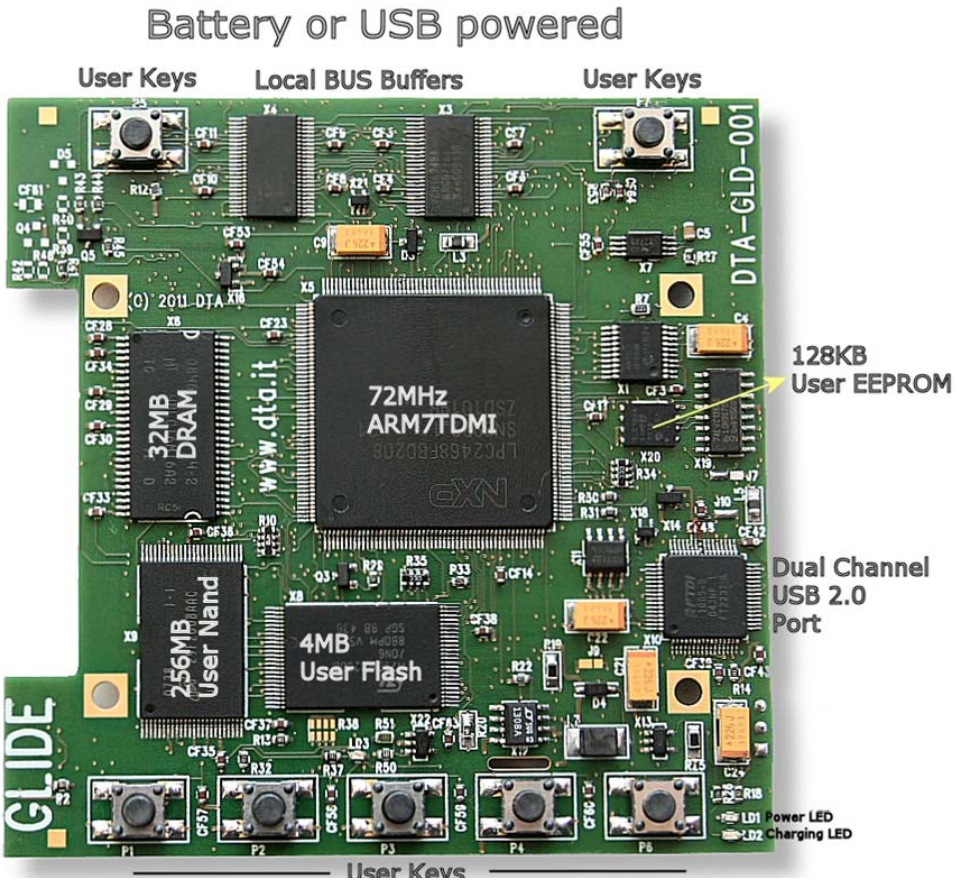
GLIDE is a board that has been created specifically for the development of battery powered instruments, complete with touchscreen display, SD and USB connection.
As a matter of fact, GLIDE works with LiION batteries that can be easily recharged through an USB connection.
The TFT QVGA (320x240) touchscreen display allows the writing of applications with a high interaction capacity.
GLIDE is equipped with Secure Digital thanks to which the board has large mass memory (FAT32) at its disposal.
The free of charge software (GPACK) allows the writing of applications with an efficient graphic interface without the need to use heavy operating systems, but with the possibility to fully apply the ARM processor resources.
The USB2 interface allows easy connection to personal computer with almost all operating systems: it is based on a FTDI (FT2232) chip that offers a serial (COM) and a fast transfer data channel to the PC.
USB also allows to update the firmware or the external FLASH used by GUI.
The board is completed with a 16 bit buffered ARM bus, a 128 Kbyte EEPROM memory and a 256 Mbyte NAND.

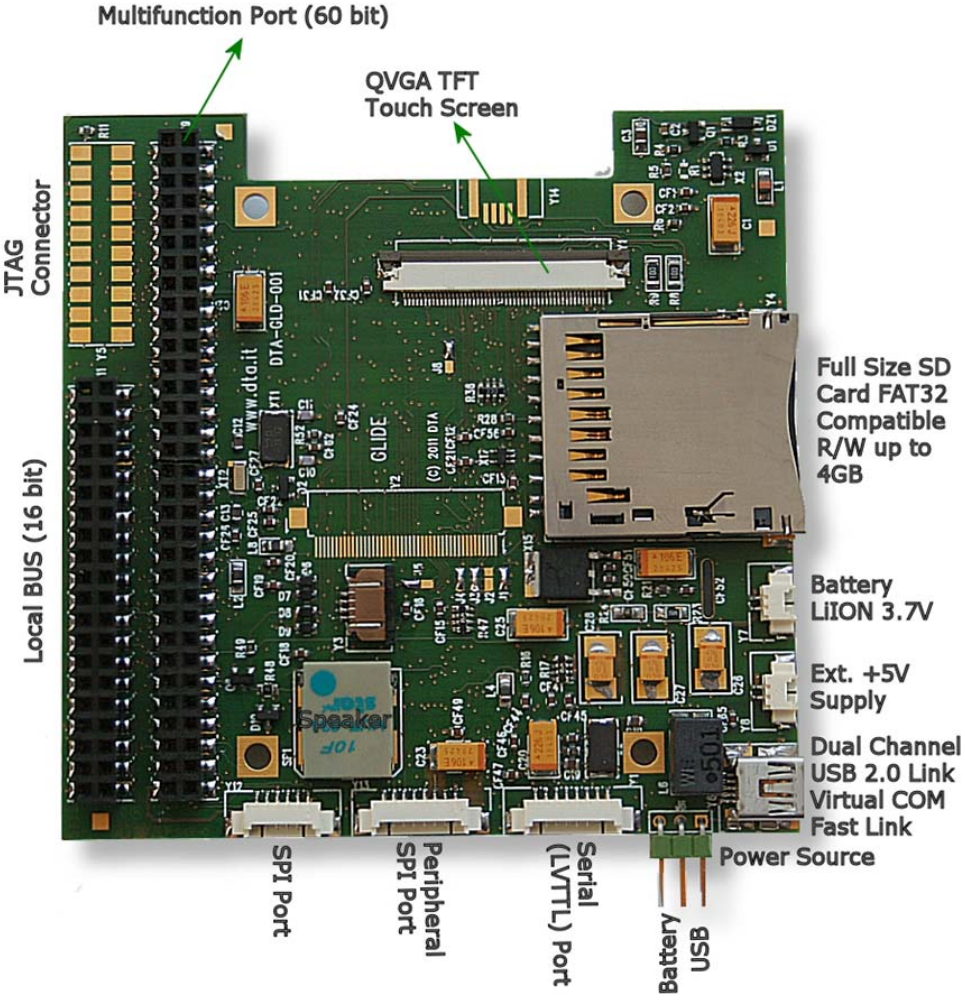
Rev. 0 Information furnished by OT is believed to be accurate and reliable. However, no responsibility is assumed by OT for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of OT Trademarks and registered trademarks are the property of their respective companies.

Via G. Cei 67, 56021 Cascina, PISA - ITALY
www.officinaturini.com
© OT, All Rights Reserved
Tel: +39 050 8665471

GLIDE

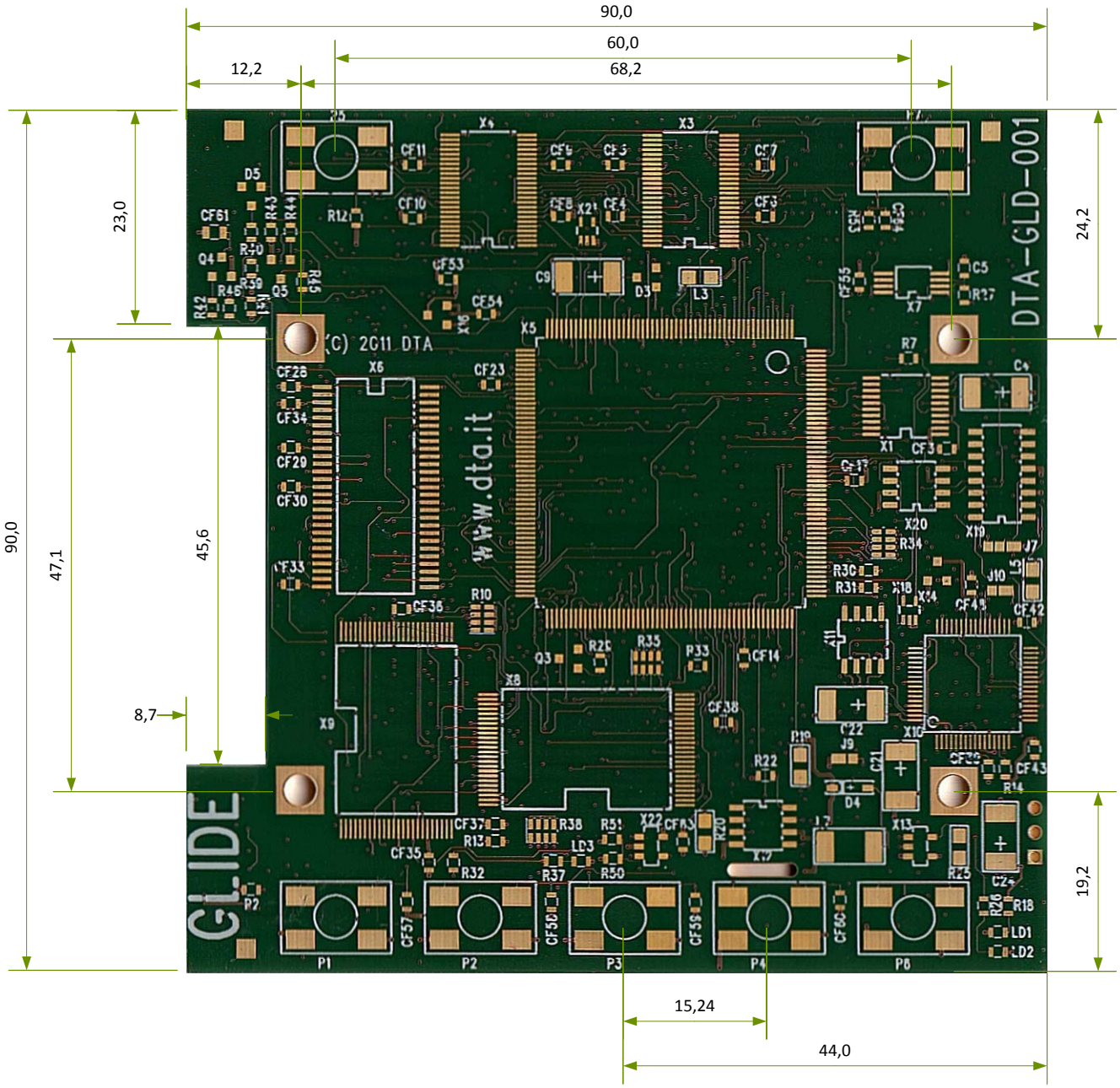
OVERVIEW





GLIDE

MECHANICAL (mm)



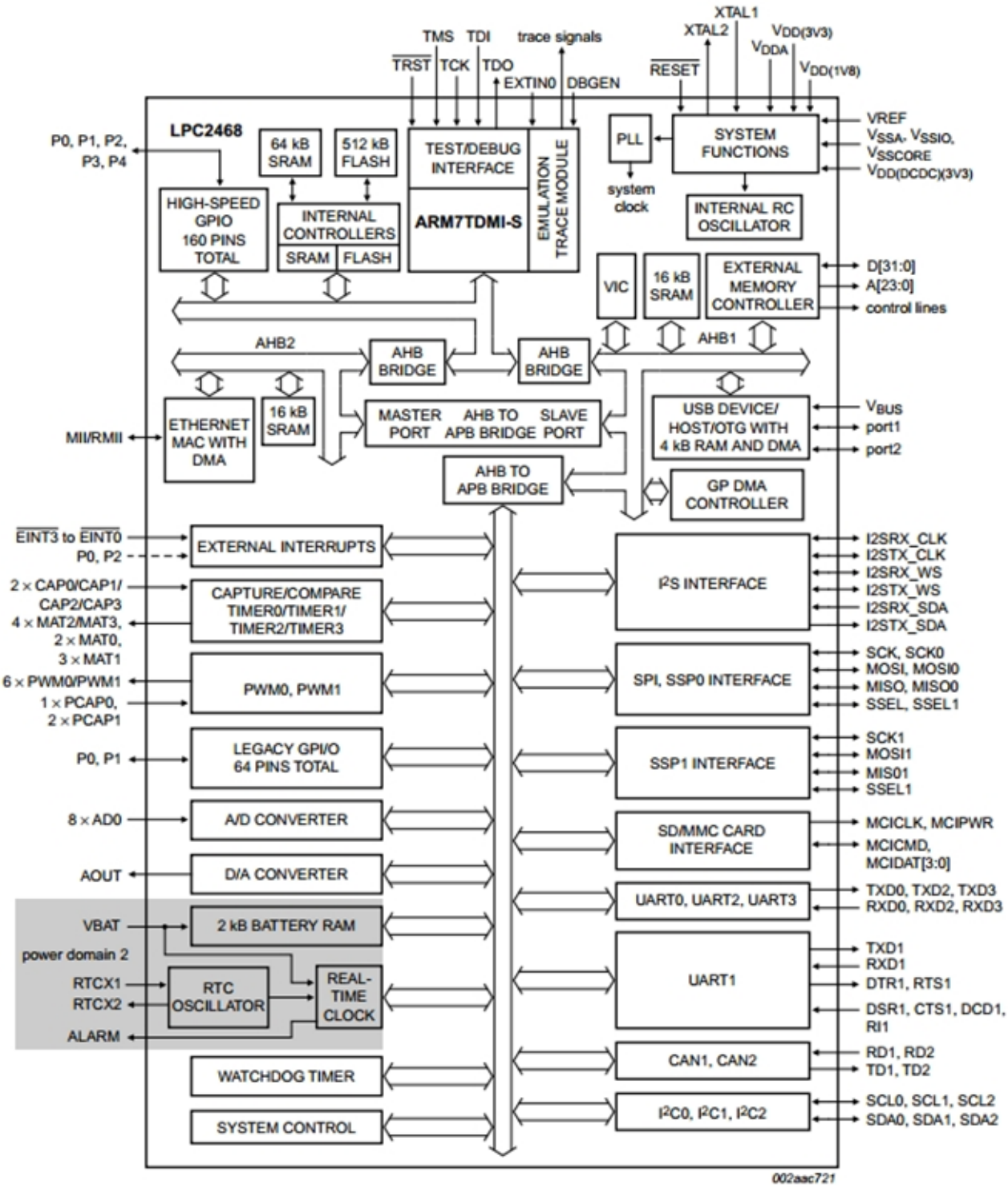


Fig 1. LPC2468 block diagram

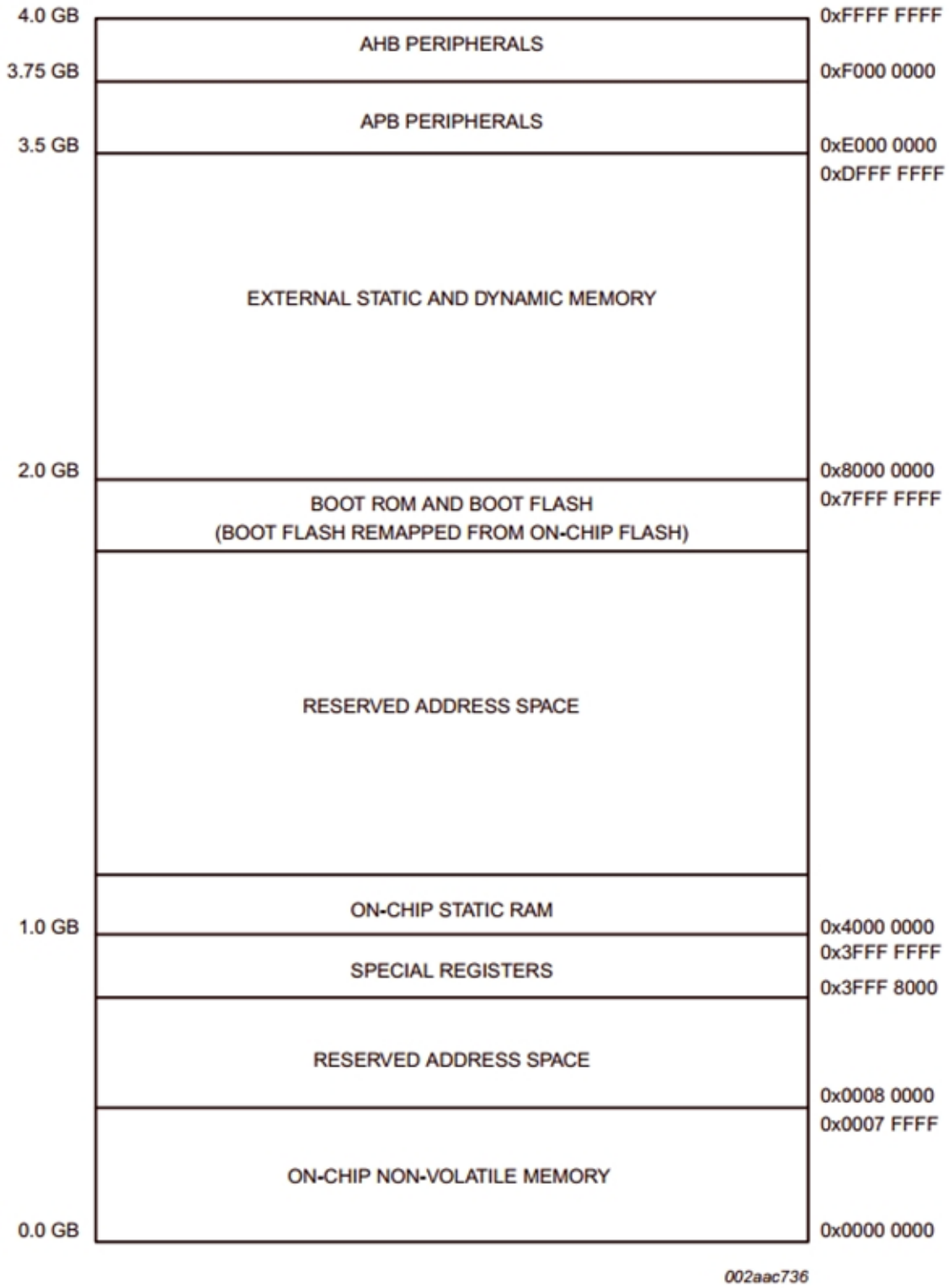


Fig 4. LPC2468 memory map

Y11 EXPANSION BUS (Buffered 16bit)

SIGNAL	PIN	PIN	SIGNAL
#RESET	**1**	**2**	+3.3V
#CS0	**3**	**4**	#CS1
DB0	**5**	**6**	DB1
DB2	**7**	**8**	DB3
DB4	**9**	**10**	DB5
DB6	**11**	**12**	DB7
DB8	**13**	**14**	DB9
DB10	**15**	**16**	DB11
DB12	**17**	**18**	DB13
DB14	**19**	**20**	DB15
#RD	**21**	**22**	#WR
A0	**23**	**24**	A1
A2	**25**	**26**	A3
A4	**27**	**28**	A5
A6	**29**	**30**	A7
A8	**31**	**32**	A9
A10	**33**	**34**	P2.19
P2.25	**35**	**36**	P2.0
P2.21	**37**	**38**	P2.13
GND	**39**	**40**	GND

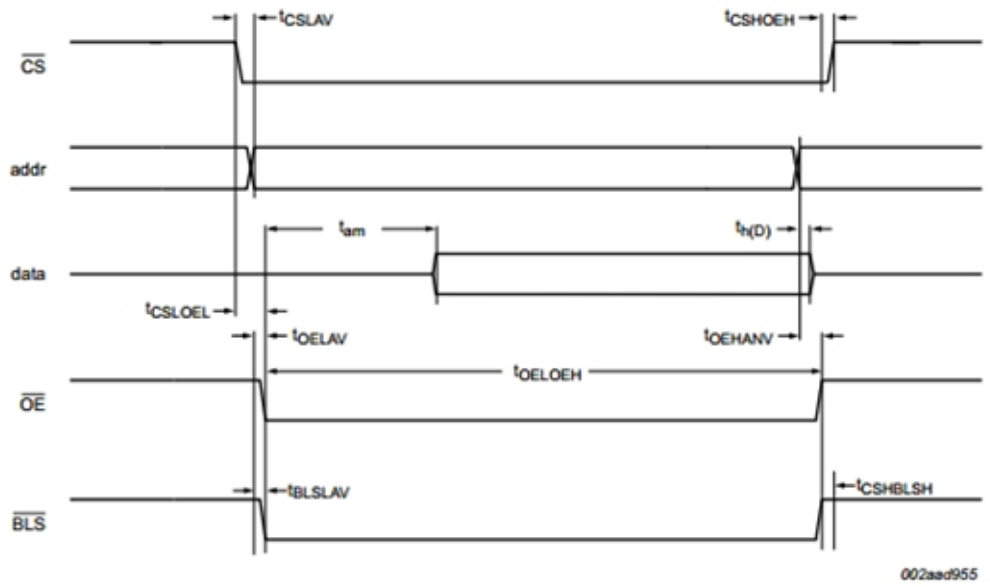


Fig 14. External memory read access

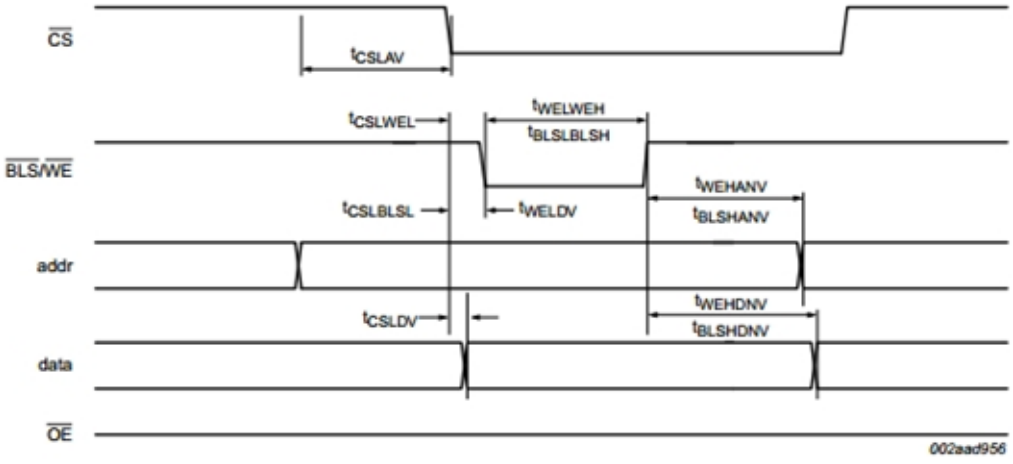
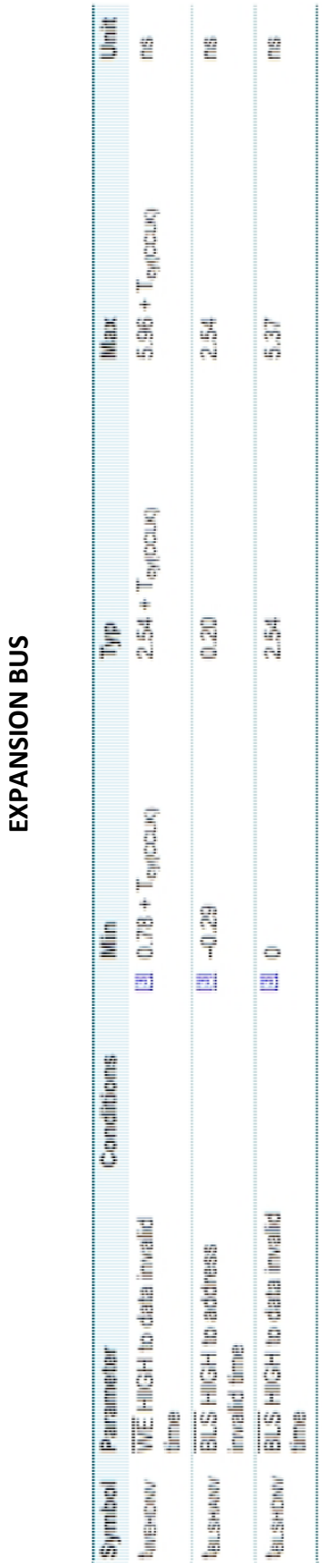


Fig 15. External memory write access

EXPANSION BUS


EXPANSION BUS

Y9 MCU PORTS

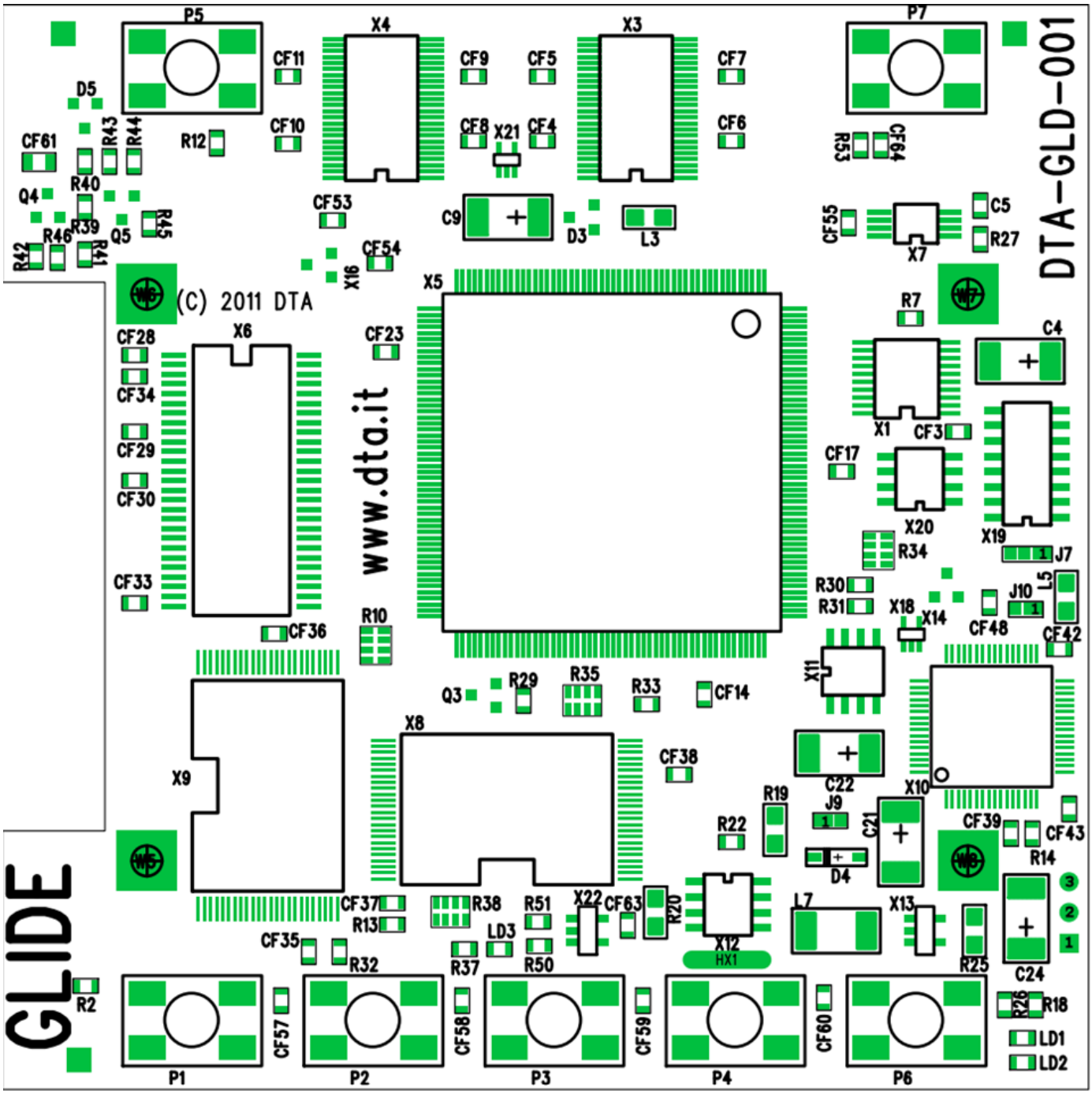
GBUS	11	10	01	00	PIN	PIN	00	01	10	11	GBUS
+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	1	2	+5V	+5V	+5V	+5V	+5V
TXD3	SDA1	TXD3	-	P0.0	3	4	P3.16	D16	PWM0[1]	TXD1	DB[0]
RXD3	SCL1	RXD3	-	P0.1	5	6	P3.17	D17	PWM0[2]	RXD1	DB[1]
TXD0	-	-	TXD0	P0.2	7	8	P3.18	D18	PWM0[3]	CTS1	DB[2]
RXD0	-	-	RXD0	P0.3	9	10	P3.19	D19	PWM0[4]	DCD1	DB[3]
DIRL	CAP2[0]	-	I2SRX_CLK	P0.4	11	12	P3.20	D20	PWM0[5]	DSR1	DB[4]
DIRH	CAP2[1]	-	I2SRX_WS	P0.5	13	14	P3.21	D21	PWM0[6]	DTR1	DB[5]
SSEL	MAT2[0]	SSEL1	I2SRX_SDA	P0.6	15	16	P3.22	D22	PCAP0[0]	RI1	DB[6]
SCK	MAT2[1]	SCK1	I2STX_CLK	P0.7	17	18	P3.23	D23	CAP0[0]	PCAP1[0]	DB[7]
MISO	MAT2[2]	MISO1	I2STX_WS	P0.8	19	20	P3.24	D24	CAP0[1]	PWM1[1]	DB[8]
MOSI	MAT2[3]	MOSI1	I2STX_SDA	P0.9	21	22	P3.25	D25	MAT0[0]	PWM1[2]	DB[9]
CK[0]	MAT3[0]	SDA2	TXD2	P0.10	23	24	P3.26	D26	MAT0[1]	PWM1[3]	DB[10]
CK[1]	MAT3[1]	SCL2	RXD2	P0.11	25	26	P3.27	D27	CAP1[0]	PWM1[4]	DB[11]
CK[2]	AD0[6]	MISO1	#USB_PPWR2	P0.12	27	28	P3.28	D28	CAP1[1]	PWM1[5]	DB[12]
CK[3]	AD0[7]	MOSI1	USB_UP_LED2	P0.13	29	30	P3.29	D29	MAT1[0]	PWM1[6]	DB[13]
SS[0]	SSEL1	USB_CONNECT2	#USB_HSTEN2	P0.14	31	32	P3.30	D30	MAT1[1]	RTS1	DB[14]
SS[1]	SCK	SCK0	TXD1	P0.15	33	34	P3.31	D31	MAT1[2]	-	DB[15]
SS[2]	SSEL	SSEL0	RXD1	P0.16	35	36	P2.0	PWM1[1]	TXD1	TRACECLK	TXD1
SA[0]	MISO	MISO0	CTS1	P0.17	37	38	P2.1	PWM1[2]	RXD1	PIPESTAT0	RXD1
SA[1]	MOSI	MOSI0	DCD1	P0.18	39	40	P2.2	PWM1[3]	CTS1	PIPESTAT1	PWM[0]
SA[2]	SDA1	MCICLK	DSR1	P0.19	41	42	P2.3	PWM1[4]	DCD1	PIPESTAT2	PWM[1]
BA[0]	SCL1	MCICMD	DTR1	P0.20	43	44	P2.4	PWM1[5]	DSR1	TRACESYNC	SY[0]
BA[1]	RD1	MCIPWR	RI1	P0.21	45	46	P2.5	PWM1[6]	DTR1	TRACEPKT0	SY[1]
BA[2]	TD1	MCIDAT0	RTS1	P0.22	47	48	P2.6	PCAP1[0]	RI1	TRACEPKT1	SY[2]
ADC[0]	CAP3[0]	I2SRX_CLK	AD0[0]	P0.23	49	50	P2.7	RD2	RTS1	TRACEPKT2	#GENA
ADC[1]	CAP3[1]	I2SRX_WS	AD0[1]	P0.24	51	52	P2.8	TD2	TXD2	TRACEPKT3	TXD2
ADC[2]	TXD3	I2SRX_SDA	AD0[2]	P0.25	53	54	P2.9	USB_CONNECT1	RXD2	EXTIN0	RXD2
ADC[3]	RXD3	AOUT	AD0[3]	P0.26	55	56	P2.10	#EINT0	#BOOT	-	#EINT[0]
SDA0	-	-	SDA0	P0.27	57	58	P2.11	#EINT1	MCIDAT1	I2STX_CLK	#EINT[1]
SCL0	-	-	SCL0	P0.28	59	60	P0.31	USB_D+2	-	-	BS[2]
BS[0]	-	-	USB_D+1	P0.29	61	62	P0.30	USB_D−1	-	-	BS[1]
#RESET	#RESET	#RESET	#RESET	#RESET	63	64	GND	GND	GND	GND	GND

MCU PORTS

SIGNAL	DIRECTION (GLIDE SIDE)	DESCRIPTION
BS[2:0]	OUTPUT	Parallel **B**us **S**election
BA[3:0]	OUTPUT	Parallel **B**us peripheral **A**ddress
SS[2:0]	OUTPUT	**S**PI channel **S**election 0-7
SA[3:0]	OUTPUT	**S**PI peripheral **A**ddress selection
CK[3:0]	OUTPUT	**C**loc**K** or strobes
SY[2:0]	INPUT	Input **SY**nc
#EINT[1:0]	INPUT	Active Low **E**xternal Interrupt
DB[15:0]	BIDIR	8/16 bit Bidirectional parallel bus
DIRL,DIRH	OUTPUT	Bus Direction = High Level: Data Transmitted from GLIDE Bus to Peripheral Bus (245 A->B)
#GENA	OUTPUT	Active Low GBUS Enable. All connected peripherals are selectable when this signal is active.
		Signal under user control.
		Fixed signals
		Power supply

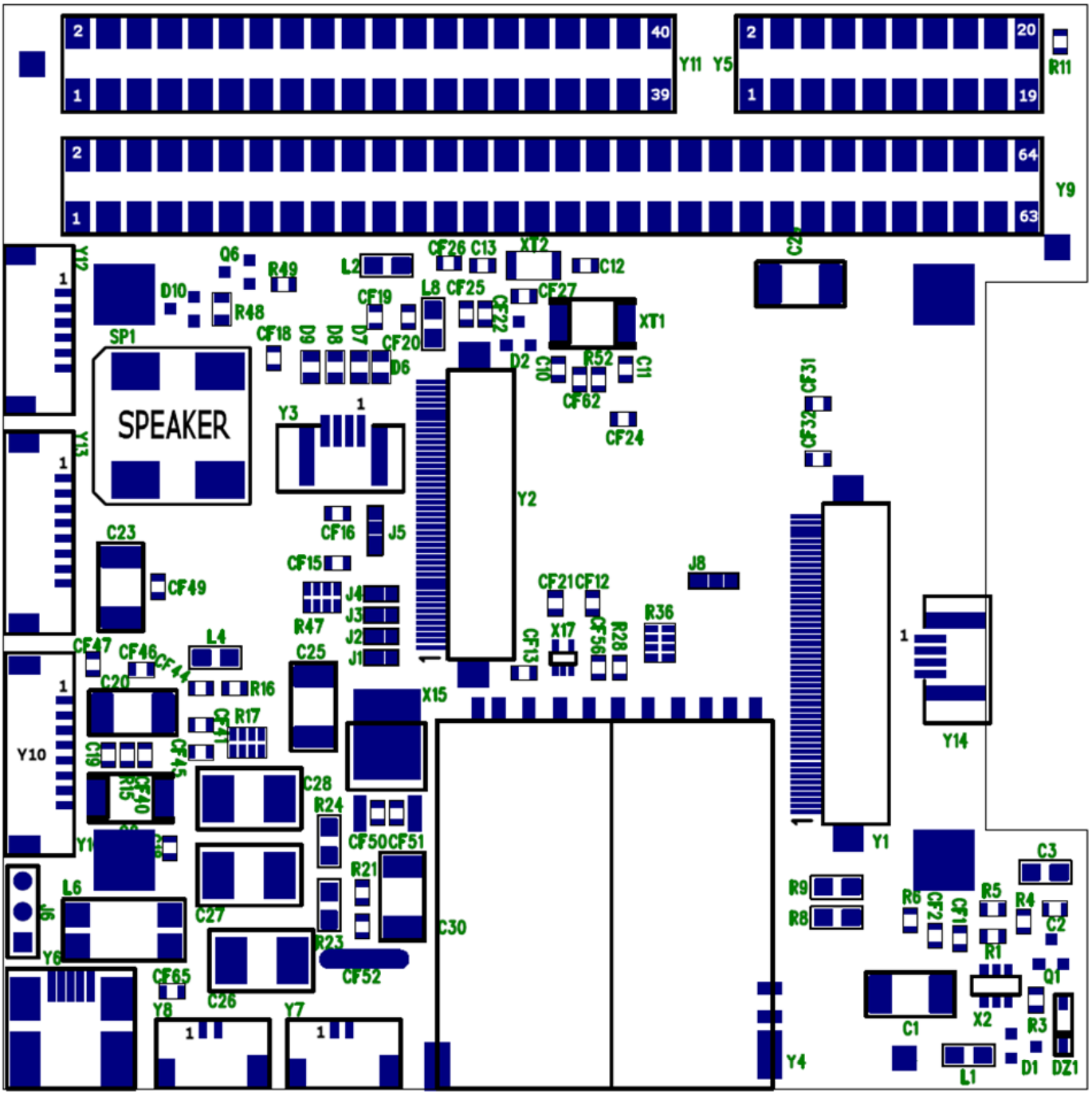
GLIDE

SILKSCREEN TOP



GLIDE

SILKSCREEN BOTTOM



GLIDE

I/O CONNECTORS

Y10		
PIN	**SIGNAL**	**DESCRIPTION**
1	+3.3V	Max 100mA
2	RTS	Serial handshake
3	/BOOT	Signal used for firmware upload (active low)
4	DTR	Serial handshake
5	/RESIN	Signal used for firmware upload
6	RXD0	Serial receive
7	TXD0	Serial transmit
8	GND	

Y12		
PIN	**SIGNAL**	**DESCRIPTION**
1	+3.3V	Max 100mA
2	/SEL	SPI select (active low)
3	SCK	SPI Clock
4	MISO	Master Input Slave Output
5	MOSI	Master Output Slave Input
6	GND	

Y13		
PIN	**SIGNAL**	**DESCRIPTION**
1	MISO	Master Input Slave Output
2	MOSI	Master Output Slave Input
3	SCK	SPI Clock
4	/P1.27	Bit port, external decode enable (active low)
5	/SEL	SPI select (active low)
6	P1.28	Decoder address
7	P1.29	Decoder address
8	GND	

Y7		
PIN	**SIGNAL**	**DESCRIPTION**
1	BATTERY	Positive LiION battery (charge 200mA)
2	GND	

Y8		
PIN	**SIGNAL**	**DESCRIPTION**
1	+5V	+5V Input or output according with J6
2	GND	

© 2012-2019 OT, All rights reserved. Trademarks and registered trademarks are the property of their respective companies.