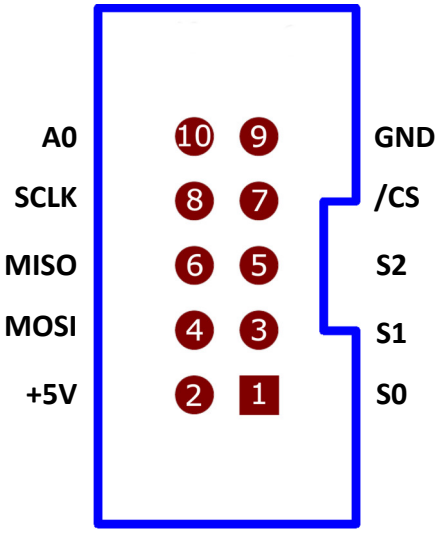
Extended SPI

ESPI

GENERAL DESCRIPTION

ESPI is a synchronous serial bus based on the SPI interface to which some control signals have been added.
It is made to be able to control up to eight peripherals placed up to a distance of 50 cm and with a maximum transmission speed of 5MHz.
Peripherals can have repeaters in order to have longer cable lengths.
All signals are LVTTL.



TE Connectivity AMP Connectors
2-1761603-3

SIGNAL DESCRIPTION

S[2:0]	Coded peripheral selection
/CS	Enable activities on the bus. Active low.
A0	Peripheral address
SCLK	Serial clock
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
+5V	Bus power

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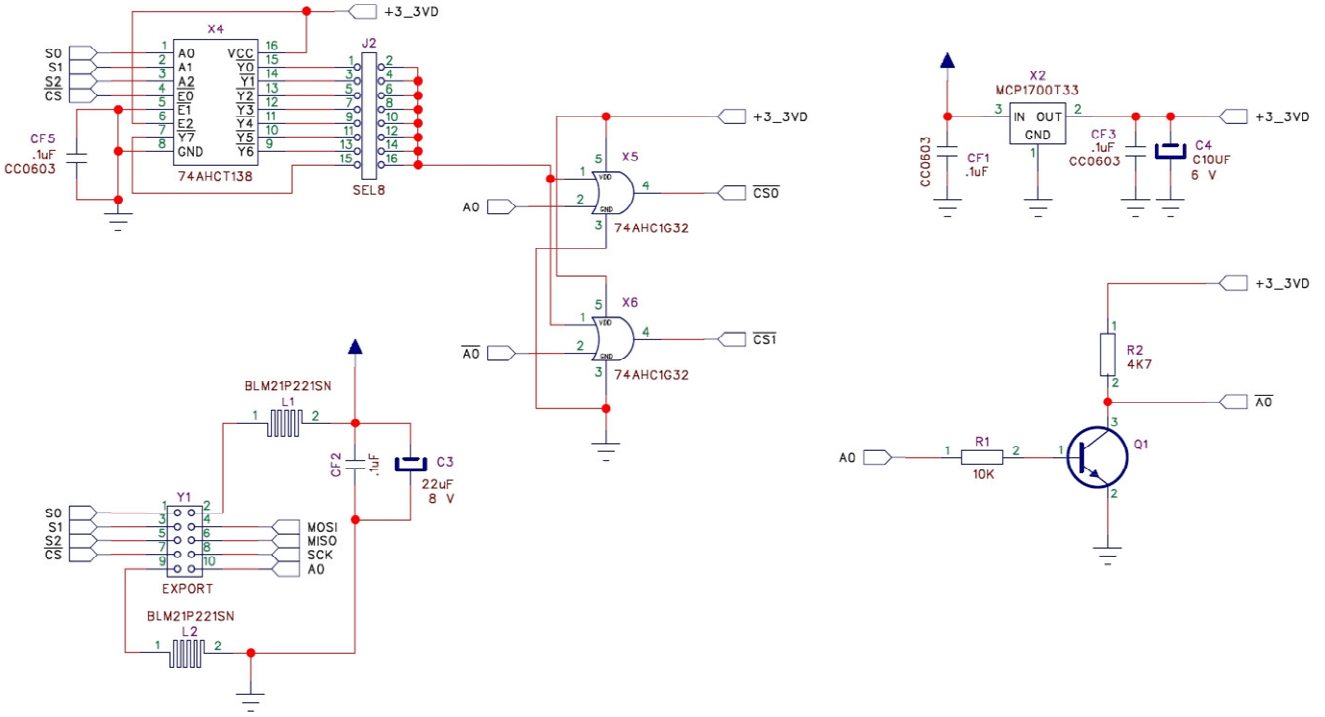
TIPICAL HARDWARE FOR ESPI PERIPHERAL



OPERATION (From Wikipedia)

To begin a communication, the bus master first configures the clock, using a frequency less than or equal to the maximum frequency the slave device supports. Such frequencies are typically up to a few MHz.

The master then transmits the logic 0 for the desired chip over the chip select line. A logic 0 is transmitted because the chip select line is active low, meaning its off state is a logic 1; on is asserted with a logic 0. If a waiting period is required (such as for analog-to-digital conversion), then the master must wait for at least that period of time before starting to issue clock cycles.

During each SPI clock cycle, a full duplex data transmission occurs:

- the master sends a bit on the MOSI line; the slave reads it from that same line
- the slave sends a bit on the MISO line; the master reads it from that same line

Not all transmissions require all four of these operations to be meaningful, but they do happen.

Transmissions normally involve two shift registers of some given word size, such as eight bits, one in the master and one in the slave; they are connected in a ring. Data is usually shifted out with the most significant bit first, while shifting a new least significant bit into the same register. After that register has been shifted out, the master and slave have exchanged register values. Then each device takes that value and does something with it, such as writing it to memory. If there is more data to exchange, the shift registers are loaded with new data[1] and the process repeats.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops toggling its clock. Normally, it then deselects the slave.

Transmissions often consist of 8-bit words, and a master can initiate multiple such transmissions if it wishes/needs. However, other word sizes are also common, such as 16-bit words for touchscreen controllers or audio codecs or 12-bit words for many digital-to-analog or analog-to-digital converters.

Every slave on the bus that has not been activated using its chip select line must disregard the input clock and MOSI signals, and must not drive MISO. The master must select only one slave at a time.